The Impact of Load SWR on the Efficiency of Power Amplifiers

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The efficiency of a power amplifier impacts the high-level system design in three ways: the power supply design, the thermal design, and the mechanical design of the overall package. As the efficiency of a power amplifier increases, the power supply can be smaller, the heat sink can be smaller, and thus the overall power amplifier package can be smaller. These three issues directly impact the cost of a power amplifier.

For many years significant effort has been expended in increasing the efficiency of a power amplifier. Power amplifier designers have gone from accepting the performance of Class C, Class B, and Class AB power amplifiers in the old days to a myriad of classes of operation to improve efficiency: Class D, Class E, Class F, Class E/F, Class S, several others, and variations thereof [reference 1]. Additionally, much work has been done in efficiency enhancement techniques: the Doherty amplifier, Chireix's outphasing amplifier, envelope elimination and restoration, and variations of these techniques [reference 2]. All of these improvements in efficiency depend upon a carefully controlled load for the amplifier.

In a laboratory environment, achieving high efficiency in a power amplifier is relatively easy. This is so because the power amplifier is usually working over a small range of frequencies (the 40m CW band, for example) into a resistive load (50 + j0 Ω). In the real world, though, the amplifier may have to work over a wider range of frequencies (most of the author's power amplifier experience is from 30 – 512MHz) and the load is a real-world antenna that can have a SWR quite a bit greater than 1:1 (for example, the power amplifiers used in the aforementioned 30-512MHz frequency range are typically required to drive an antenna SWR as high as 3:1). The purpose of this article is to show how the efficiency of a power amplifier varies as the load SWR phase angle varies.

The effect of variable load SWR will be examined with computer modeling. To begin, the modeled performance of a power amplifier driving a 50Ω load will be compared to the measured data of the actual power amplifier driving 50Ω to gain confidence in the model. Then the model will be used to assess the impact of load SWR on the drain efficiency of the power amplifier. Finally, techniques to mitigate efficiency degradation due to load SWR will be discussed.

The Power Amplifier

The power amplifier modeled appeared in the January/February 2004 issue of *QEX* [reference 3]. It is a 200w Class E/F high efficiency design, and it uses a pair of International Rectifier IRFP044N power MOSFETs. It is designed for 40m CW and a nominal 12.8v power supply. From Figure 5 in the *QEX* article, the power amplifier delivered 200w to a 50Ω load at 5w input (16dB gain) at a drain efficiency around 80%.

The Model

The modeling was done using harmonic balance simulation in Agilent Technologies Advanced Design System (ADS) 2003C software. The model of the power amplifier driving a 50Ω load is shown in Figure 1, which is on the last page of this article.

The schematic for the power amplifier model came from Figure 3 in the *QEX* article. There were some errors in the original *QEX* article, and these were corrected in subsequent issues (Mar/Apr 2004 p61, May/June 2004 p61-62, and Jul/Aug 2004 p61).

The model of each IRFP044N MOSFET came from International Rectifier's website [footnote 1]. The IRFP044N model is a SPICE model, and it was imported into ADS without difficulty. The gate bias on the IRFP044N MOSFETs was set to 3.5v, as given in the *QEX* article.

Parameters for the passive components mostly came from the *QEX* article (and the subsequent corrections) and from the respective component data sheets. If data was not given in the article or was not available from vendor data sheets (for example, inductor loss data), it was estimated based on the author's experience with power amplifiers. A frequency of 7.025MHz was chosen for the model.

ADS Data Display Screen

Figure 2 is a typical ADS data display screen with several pertinent parameters displayed.

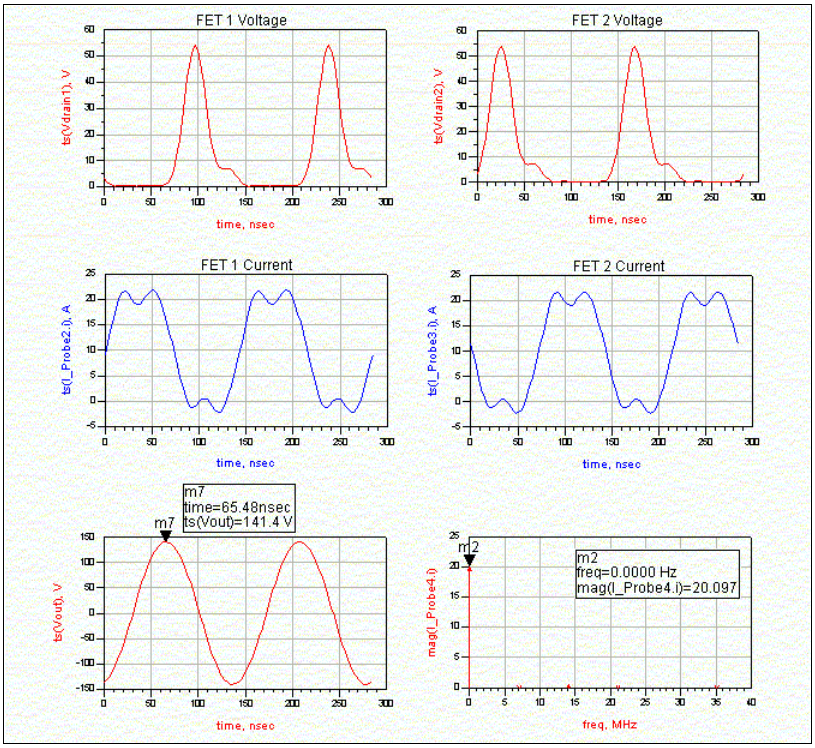


Figure 2 - Typical ADS Screen

The two upper panels show the drain voltage pulse at each IRFP044N. Note that the two IRFP044Ns are operating in push-pull (the time difference between the first pulse in the FET 1 Voltage curve and the first pulse in the FET 2 Voltage curve is 71nsec, which corresponds to 180^{o} at 7.025MHz).

The two middle panels show the drain current pulse at each IRFP044N. Note that there is very little overlap in the drain current pulse and the drain voltage pulse (from the upper panel) for either transistor. In other words, the drain current pulse (I) and the drain voltage pulse (V) do not occur simultaneously. With a minimal I x V product across the transistor at any given time, the dissipative loss in either IRFP044N is low and the result is high efficiency [footnote 2].

The bottom left panel is the voltage across the load (Term2 in Figure 1). It is used to calculate the power into the load. The m7 marker is a peak voltage, so it has to be multiplied by .707 to calculate the rms voltage. This is then used to calculate the average power delivered to the load.

The bottom right panel shows the supply current (marker m2) from the 12.8v source (SRC1 in Figure 1). This is used to calculate the drain efficiency of the power amplifier using the equation:

$$\text{Drain efficiency} = \frac{\text{average power delivered to load}}{\text{12.8V x supply current}}$$

Performance: Modeled versus Measured

In the model, the input power Pin was varied from 1w to 20w, and the simulated output power Pout and simulated drain efficiency were recorded. This data is plotted in Figures 3 and 4 (larger versions are at the end of this article), along with the measured data from the *QEX* article.

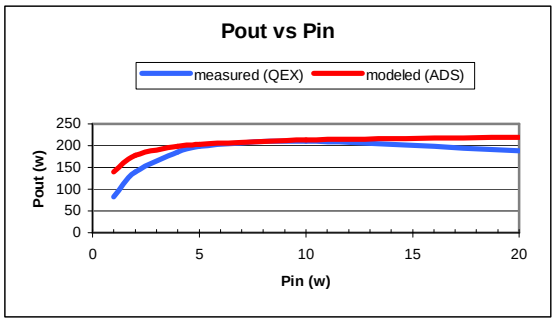


Figure 3 – Comparison of Pout vs Pin

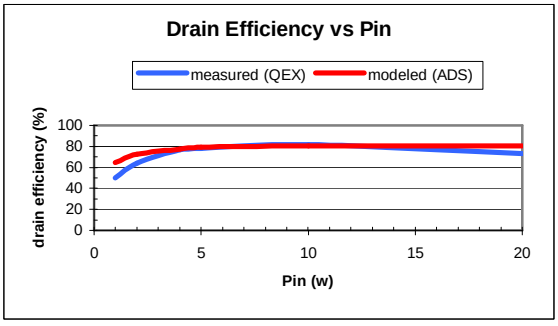


Figure 4 – Comparison of Efficiency vs Pin

As can be seen in Figures 3 and 4, the modeled Pout versus Pin curve and the modeled Drain Efficiency versus Pin curve compare favorably to the measured data.

The 50Ω data taken from the model is shown in Table 1, and serves as a reference for the SWR data that follows. The assumptions used to calculate the data in Table 1 follow the table.

Load impedance	Drain current	Drain efficiency	Power delivered to load	Power dissipated (waste heat)	IRFP044N flange temperature	IRFP044N junction temperature
50 + j0	20.1a	77.7%	200w	57w	50°C	68°C

Table 1 – Baseline 50Ω Performance (Model)

1. Drain voltage = 12.8v
2. Push-pull operation
3. Junction-to-case thermal resistances = 1.3°C/W (from IRFP044N data sheet)
4. Case-to-sink thermal resistance = 0.24°C/W (from IRFP044N data sheet)
5. Sink-to-ambient thermal resistance = 1.5°C/W (3 inch by 3 inch heat sink with 1.5 inch long fins using 250 ft/min forced air)
6. Ambient temperature = +25°C
7. 50% duty cycle (from *QEX* article)

With assurance from Figures 3 and 4 that the model satisfactorily emulates the actual power amplifier, operation into a mismatched load was simulated next.

Choosing a Practical Load SWR

Since the high efficiency *QEX* power amplifier was designed for 40m CW, a horizontal 40m dipole at 50 feet over average ground using #12 wire was modeled. The antenna was designed to resonate at the center of the 40m band (7.150MHz). Analysis using NEC 2.0 [footnote 3] yields a resistance at resonance of 86.6Ω, which is a SWR of 1.73:1. The SWR rises to around 2:1 at each end of the band.

Since the *QEX* power amplifier was designed and modeled for 40m CW at the low end of the band, the SWR used to evaluate the power amplifier efficiency will be 2:1 at all phase angles (to emulate any length of transmission line from the dipole to the power amplifier). Loss in the length of transmission line is ignored. In real HF applications the loss would be small and would slightly reduce the SWR seen by the power amplifier.

This analysis is similar to a "load pull" measurement often performed on real hardware to learn its response to a non-50Ω load in which the phase angle is varied.

Effect of Load SWR

The power amplifier performance into a 2:1 SWR was simulated by using a load with a reflection coefficient magnitude of 0.333 at eight discrete phase angles: 0°, -45°, -90°, -135°, -180°, +135°, +90°, and +45°. The infinite number of phase angles necessary to simulate *any* length of transmission line is reduced to only 8 discrete angles separated by 45° to simplify a very time consuming exercise. The results are more than sufficient to illustrate the effect of varying the SWR phase angle. The input power was held constant

at 5w. The result of this exercise is shown in Table 2. The column 'power delivered to the load' is the power into the resistive part of the load impedance.

Reflection coefficient	Load impedance	Drain current	Drain efficiency	Power delivered to load	Power dissipated (waste heat)	IRFP044N junction temperature
0.333∠0°	100 + j0	33.1a	62.3%	264w	160w	147°C
0.333∠-45°	70 – j37	32.1a	51.6%	212w	199w	176°C
0.333∠-90°	40 – j30	24.8a	48.2%	153w	164w	150°C
0.333∠-135°	28 – j15	17.8a	56.6%	129w	99w	100°C
0.333∠-180°	25 + j0	12.2a	82.6%	129w	27w	46°C
0.333∠+135°	28 + j15	11.6a	80.1%	119w	29w	47°C
0.333∠+90°	40 + j30	16.8a	63.7%	137w	78w	84°C
0.333∠+45°	70 + j37	25.5a	60.7%	198w	128w	122°C

Table 2 – Modeled Performance into a 2:1 SWR

Figures 5 and 6 (larger versions are at the end of this article) are plots of the data in Table 2 and illustrate the sinusoidal nature of the various amplifier parameters as the 2:1 load phase angle presented to the power amplifier was varied.

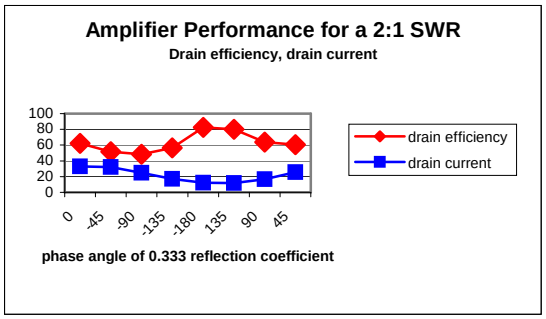


Figure 5 – Drain Efficiency and Current

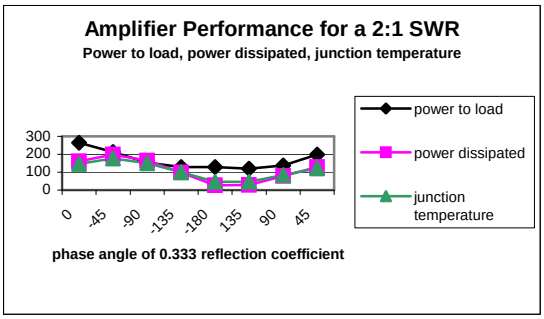


Figure 6 – Power to Load, Power Dissipated, and Junction Temperature

This sinusoidal nature is typical of what is seen with practical power amplifiers. The minimum-to-maximum excursion about the baseline of each parameter will depend on the specific power amplifier design.

Table 2 and Figures 5 and 6 show several interesting results. First, as expected, the drain efficiency varies significantly as the power amplifier is presented different impedances around a 2:1 SWR. Second, the power delivered to the load also varies significantly as the power amplifier is presented different impedances around a 2:1 SWR. Third, as a result of both the efficiency changing as the load goes around a 2:1 SWR circle and the amount of RF power produced as the load is varied, the IRFP044N junction temperature varies by more than 125°C.

There are two important issues revealed by the data in Table 2 and Figures 5 and 6, and both are the result of a load on the high impedance side of the 2:1 SWR (a reflection coefficient angle between roughly 0° and –45°). First, the current drain could easily exceed the rating of components in the power amplifier and of components in the power

supply (the IRFP044Ns are rated at 53A continuous, so the modeled 33A shouldn't be a problem). Second, the calculated junction temperature of the IRFP044N is right at its maximum junction temperature rating (175^{o}C from the IRFP044N data sheet).

To get around the high current drain issue, a bigger power supply could be designed or current limiting could be employed in the power supply design. The junction temperature issue is probably the lesser of two evils, as exceeding the 175^{o}C rating *by a small amount* is not a 'fall off the cliff' issue – it's more of a long-term reliability issue. But remember that the calculated junction temperature of 176^{o}C is for a duty cycle of 50% (from assumption 7 after Table 1). If the power amplifier is used in a data mode (RTTY, for example) at the worse case 2:1 SWR, the junction temperature would be around 327^{o}C. This is a serious problem, and something would need to be done.

Mitigating Current Drain and Junction Temperature Issues

Although using this power amplifier at a worse case 2:1 SWR at 50% duty cycle shouldn't cause any catastrophic failures, there are two approaches to mitigating increased current drain and increased junction temperature that would keep performance more constant when operated into a SWR.

If the use of a power amplifier is confined to narrow band operation (for example, 40m CW), then it would be a simple matter to prune the antenna to the desired frequency. In the case of the aforementioned horizontal dipole cut for 7.150MHz, the antenna could be physically lengthened and the wires sloped down at about a 45^{o} angle (making it into an inverted-vee). This will move the resonance down to the CW portion of the 40m band and it will also decrease the resistance at resonance to very near 50Ω – just what the high efficiency power amplifier was designed for.

If the power amplifier is used over a wider bandwidth or on several bands where the antenna(s) SWR is a compromise, then the mitigating approach would be to use an antenna tuner to always present 50 + j0 Ω to the power amplifier. This would also be the *required* solution if an ALC (automatic level control) loop is put around the power amplifier to keep its output power more constant versus antenna impedance.

If the power amplifier is for VHF and above, an isolator (or a circulator with an external 50Ω load) would be an effective method to mitigate the effects of SWR.

Conclusion

This article demonstrates that the efficiency of a power amplifier varies significantly when it is operated into a moderate SWR having an arbitrary phase angle. This degradation could place a current drain stress on the power amplifier components and/or power supply components, and possibly create excessive junction temperatures in the power amplifier active device(s).

The solution is to restrict operation to a narrow band where the antenna has been optimized, use an antenna tuner, or use an isolator (power amplifiers for VHF and above).

Acknowledgement

I'd like to thank Ed Paragi WB9RMA for his review of and suggestions to this article.

References

1. Peter B. Kenington, "High-Linearity RF Amplifier Design," Artech House, 2000.

2. Steve C. Cripps, "RF Power Amplifiers for Wireless Communications," Artech House, 1999.

3. T. Taniguchi, K. Potter KC6OKH, and D. Rutledge KN6EK, "A 200 W Power Amplifier," *QEX*, Jan/Feb 2004, pp 3-6.

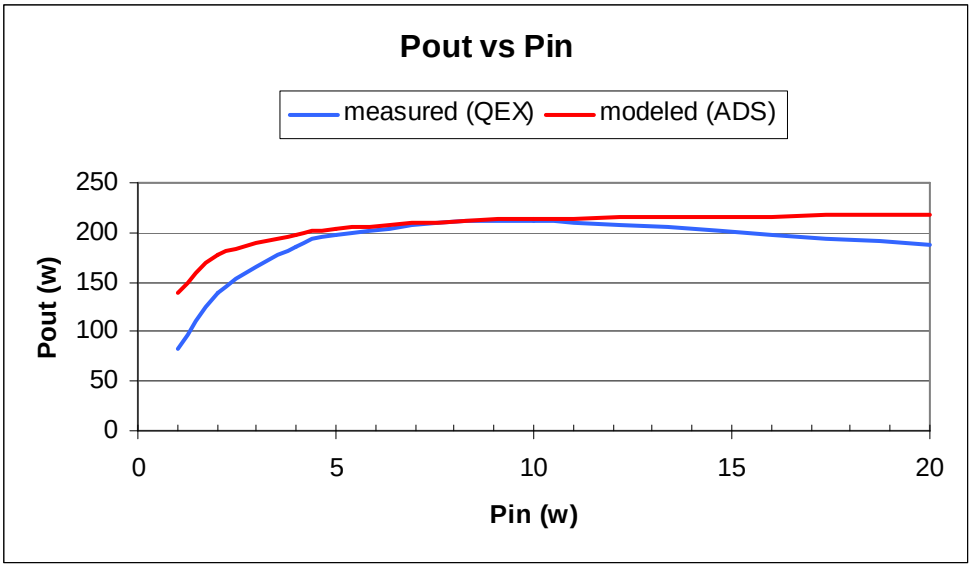
Footnotes

1. **http://www.irf.com/product-info/models/SPICE/irfp044n.spi**

2. It's important to note that the high efficiency of the *QEX* power amplifier is not because it's operating in push-pull. It's due to shaping of the drain waveforms on each transistor to minimize any overlap between the drain voltage pulse and the drain current pulse on each transistor.

3. K6STI's NEC/WIRES 2.0 software was used to simulate the dipole. W7EL's EZNEC software could also be used.

Appendix – Larger Versions of Figures 3, 4, 5, and 6



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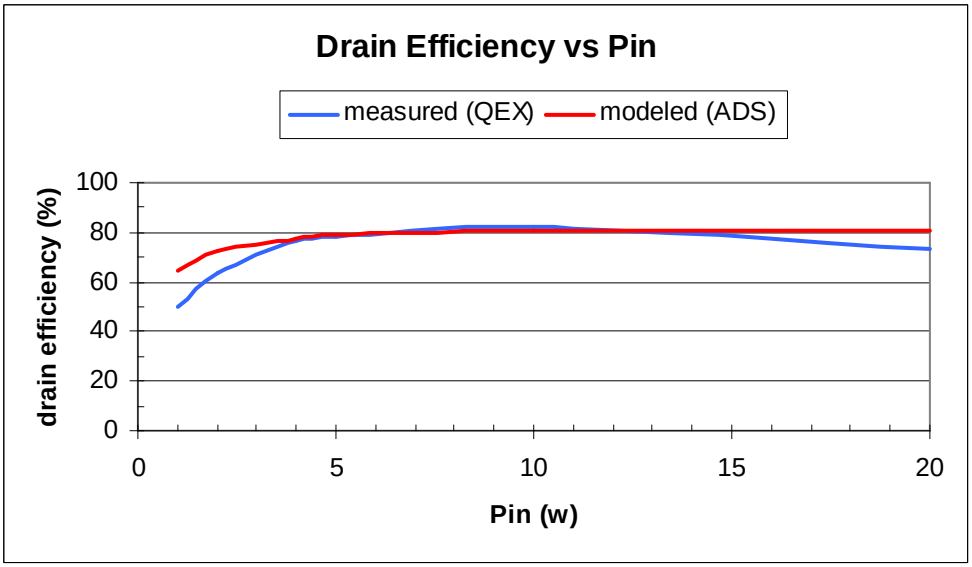

Figure 4 – Comparison of Efficiency vs Pin

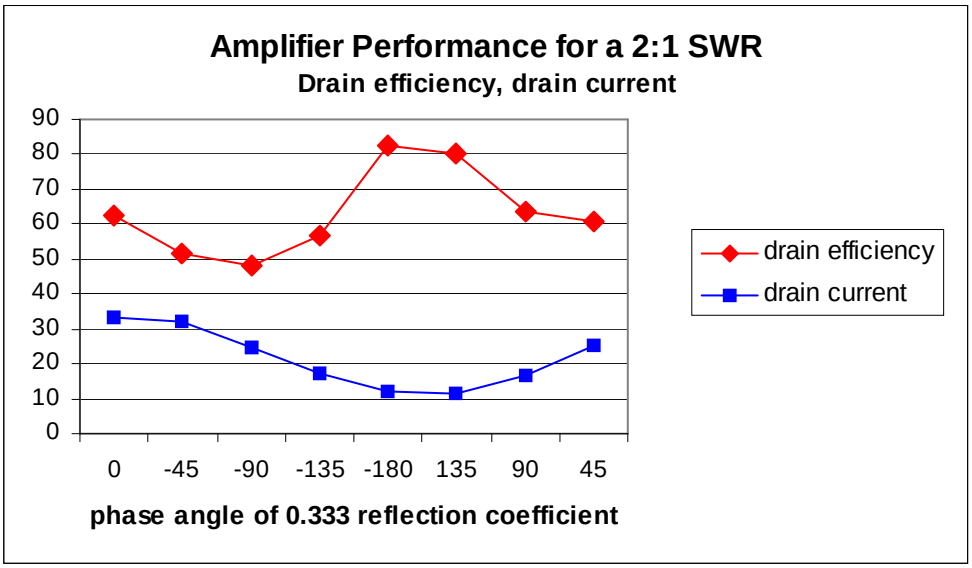

Figure 5 – Drain Efficiency and Current

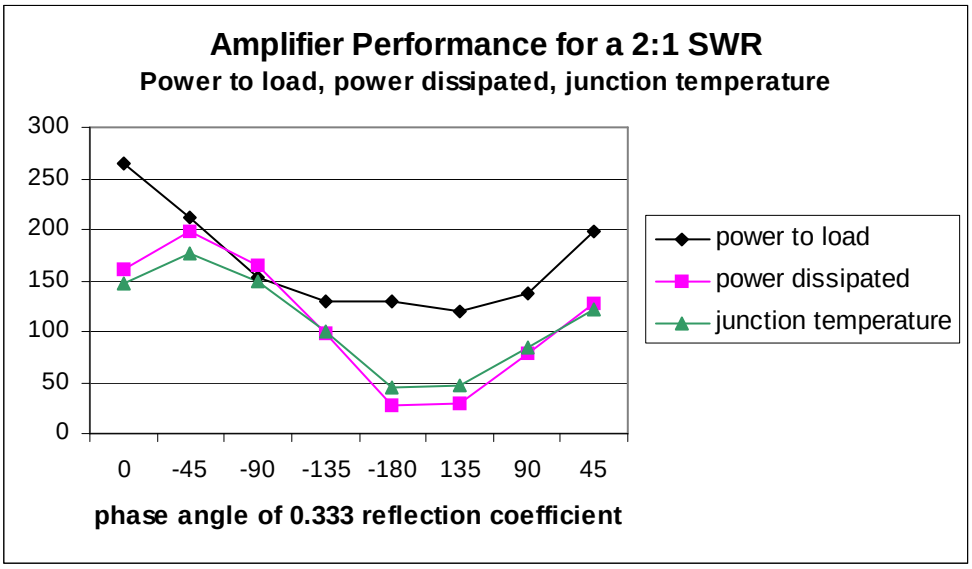

Figure 6 - Power to Load, Power Dissipated, and Junction Temperature

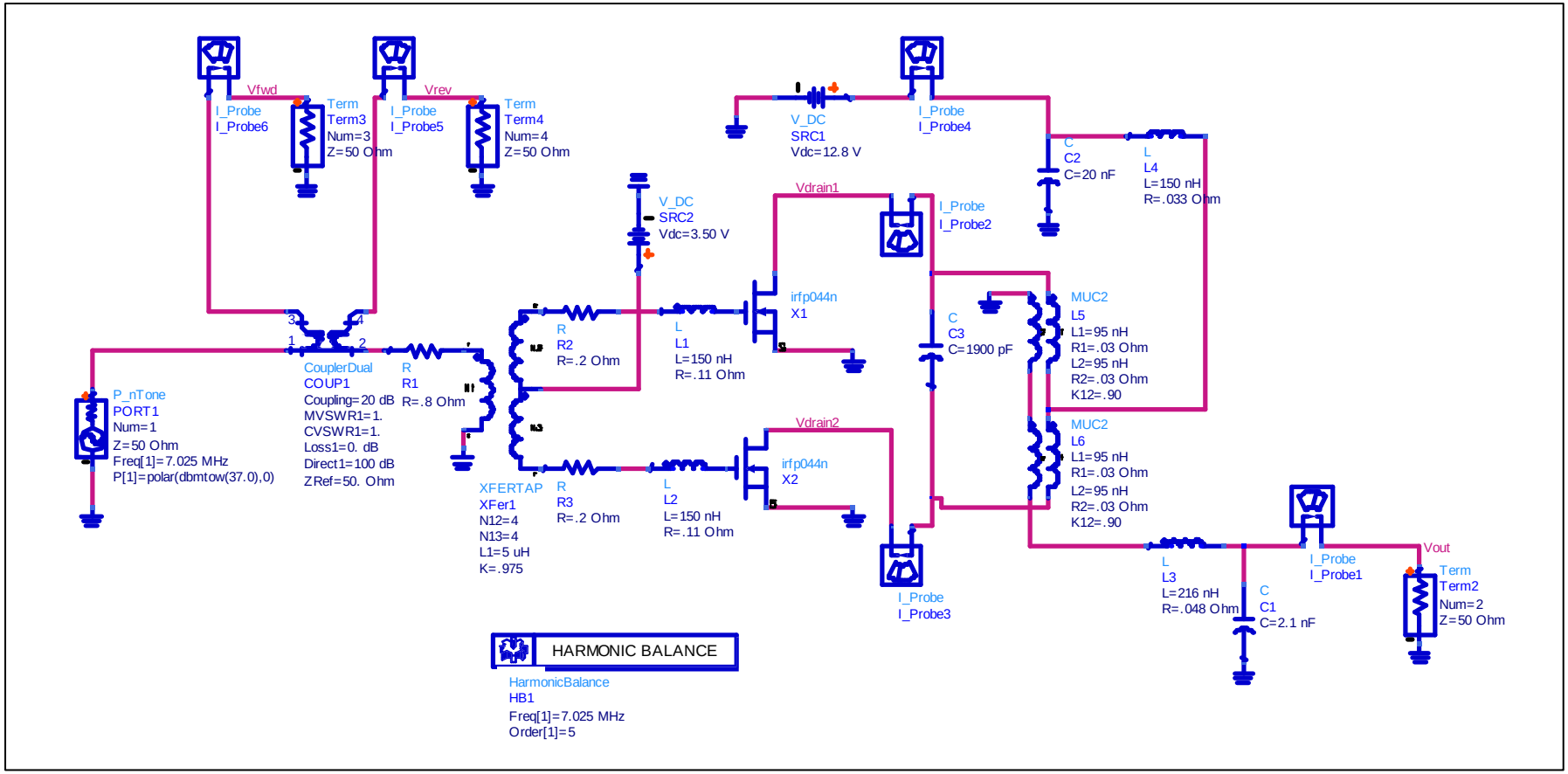

Figure 1 – ASDS Model of 200w Class E/F Power Amplifier